REMARKS

I. Status Summary

Claims 1-23 are pending in the instant application. Claims 1, 3, and 18 are amended herein. Therefore, upon entry of this Amendment, Claims 1-23 will be pending under consideration. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth herein below is respectfully requested.

II. Objections to the Drawings

The Examiner has objected to Figure 2 of the Drawings because it is missing element reference numerals. Official Action, page 2. A replacement drawing sheet for Figure 2 is submitted herewith that adds reference numerals **35-47**. The portion of the specification describing Figure 2 has been amended to include reference numerals **35-47**. In light of the proposed amendments to Figure 2 and the description of Figure 2 in the specification, it is respectfully submitted that the objection to Figure 2 should be withdrawn.

III. Claim Rejections under 35 U.S.C. § 112

Claim 3 stands rejected under 35 U.S.C. § 112, second paragraph, under the contention that the claim fails to particularly point out and distinctly claim the subject matter which applicants regard as the invention. In particular, the Examiner states that

Claim 3 recites the element "the ROM memory" in Claim 1 and that there is insufficient antecedent basis for this element in the claim. Claim 3 has been amended to replace the element "the ROM memory" with the element "a ROM memory". In view of the amendment to Claim 3, applicants submit that the claim complies with the antecedent basis requirement and that the objection should be withdrawn.

IV. Claim Rejections Under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 1-7 under 35 U.S.C. § 103(a) as being unpatentable over Applicants Admitted Prior Art (hereinafter, "AAPA") in view of U.S. Patent No. 5,706,466 to Dockser (hereinafter, "Dockser"). Official Action, page 2. Regarding Claim 1, the Examiner states that AAPA teaches a high speed processor including several of the elements recited in Claim 1 except that the data memory has "its own 'data memory address bus' to the data processing unit". Official Action, page 3. The Examiner also states that AAPA fails to disclose "the input and output interface buffers having their own 'interface address bus' connected to the data processing unit". Official Action, page 3. With regard to AAPA, the Examiner specifically refers to Figure 2 and related description in the present application. Official Action, page 3. Further, the Examiner states that Dockser teaches that "no matter how fast the processor, performance cannot be increased once the bandwidth of a bus is fully used" and that

"[t]he use of separate buses doubles the communication bandwidth in a system". Official Action, page 4. The Examiner contends that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to separate the 'address bus' disclosed in AAPA into two buses, the 'data memory address bus' and the 'interface address bus' because it increases performance and doubles the bandwidth in the system". Official Action, page 4.

Claims 2-23 depend from Claim 1. As stated above, Claim 1 has been amended to recite (1) a data memory which is connected to the data processing unit via a data bus and can be addressed by the data processing unit via a data memory address bus in a data address space; and (2) the input interface buffer and the output interface buffer being directly addressable by the data processing unit via an interface address bus in an independent interface address space. Summarily, neither AAPA nor Dockser, alone or in combination, discloses (1) a data memory which is connected to the data processing unit via a data bus and can be addressed by the data processing unit via a data memory address bus in a data address space; and (2) the input interface buffer and the output interface buffer being directly addressable by the data processing unit via an interface address bus in an independent interface address space.

Regarding AAPA, the Examiner refers to Figure 2 of the present application. AAPA discloses a single address bus **39** for addressing data memory **41** and ports **38** and **40**. Present Application, page 2, lines 2-29, and Figure 2. Additionally, the Examiner notes that data memory **41** and input and output ports **38** and **40** all connect

to address bus **39**. Official Action, page 3. On the other hand, Claim 1 recites a data memory address bus in a data address space that is separate from an interface address bus in an independent interface address space. Applicants respectfully submit that a data memory address bus in a data address space that is separate from an interface address bus in an independent interface address space is not disclosed or suggested by AAPA. Additionally, AAPA offers no suggestion to modify the system disclosed therein to arrive at the presently claimed invention.

Dockser fails to overcome the significant shortcomings of AAPA. Dockser is directed to a Von Neumann data processing system. Dockser, column 3, lines 43 and 44. The data processing system of Dockser includes a processing system having a combined instruction and data memory. Dockser, column 3, line 45. Dockser discloses that the system is constrained by the bandwidth of the data bus over which all data and instructions of the instruction and data memory must travel. Dockser, column 2, line 22-26. In contrast, Claim 1 recites a data memory address bus in a data address space that is separate from an interface address bus in an independent interface address space. This configuration recited in Claim 1 is advantageous because it increases the communication bandwidth of the system. Applicants respectfully submit that a data memory address bus in a data address space that is separate from an interface address bus in an independent interface address space is not disclosed or suggested by Dockser. Applicants respectfully submit that the teachings of Dockser does not teach or suggest each and every element of the present invention. Therefore, Claim 1 is

believed to be patentably distinguished over Dockser. Applicants respectfully request that the rejection of Claim 1 under 35 U.S.C. § 103(a) be withdrawn and the claim allowed at this time.

Claims 2-23 depend from Claim 1. Therefore, the comments presented above relating to Claim 1 apply equally to Claims 2-23. Thus, Claims 2-23 are believed to be patentably distinguished over AAPA and Dockser. Applicants respectfully request that the rejection of Claims 2-7 under 35 U.S.C. § 103(a) be withdrawn and the claims allowed at this time.

V. Conclusion

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and such action is earnestly solicited.

If any minor issues should remain outstanding after the Examiner has had an opportunity to study the Amendment and Remarks, it is respectfully requested that the Examiner telephone the undersigned attorney so that all such matters may be resolved and the application placed in condition for allowance without the necessity for another Action and/or Amendment.

Application Serial No.: 09/928,797

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

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REJ/BJO/gwc

Enclosure: Replacement Sheet for Figure 2

Customer No: 25297

1406/13